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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte STEPHEN R. VAN DOREN, GREGORY EDWARD TIERNEY, and SIMON C. STEELY JR.

Appeal 2009-002616
Application 10/760,599[1]
Technology Center 2100

Decided: September 28, 2009

Before LANCE LEONARD BARRY, JEAN R. HOMERE, and JAY P. LUCAS, *Administrative Patent Judges*.

LUCAS, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

Appellants appeal from a final rejection of claims 1-7 and 9-30 under authority of 35 U.S.C. § 134(a). Claim 8 would be allowed if put into

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[1] Application filed January 20, 2004. The real party in interest is Hewlett-Packard Development Co.

independent form (App. Br. 3, middle). The Board of Patent Appeals and Interferences (BPAI) has jurisdiction under 35 U.S.C. § 6(b).

Appellants' invention relates to a method and system for maintaining consistency of the value of variables (coherency) in a computer system with cache memory. In the words of Appellants:

> Coherency protocols have been developed to ensure that whenever a processor reads a memory location, the processor receives the correct or true data. Additionally, coherency protocols help ensure that the system state remains deterministic by providing rules to enable only one processor to modify any part of the data at any one time. If proper coherency protocols are not implemented, however, inconsistent copies of data can be generated.
>
> This disclosure relates generally to a coherency protocol that facilitates migration of an ordering (or serialization) point to memory. The coherency protocol, for example, facilitates migrating an ordering point from a processor's cache to memory in a system employing a broadcast-based protocol. Coherency of the data that is being written to memory can be ensured, for example, by causing subsequent broadcast requests for the data to retry the request. The retry can be implemented, for example, using a forward progress protocol or other forward progress techniques to ensure the request is completed, such as after the memory update has been completed in the system.

(Spec. 2, ¶ [0004]; 4, ¶ [0019]).

Claim 1 is exemplary:

> Claim 1 A system comprising:
>
> a first node that includes an ordering point for data, the first node being operative to employ a write-back transaction associated with writing the data back to memory, the first node

broadcasting a write-back message to at least one other node in the system in response to an acknowledgement provided by the memory indicating that the ordering point for the data has migrated from the first node to the memory.

The prior art relied upon by the Examiner in rejecting the claims on appeal is:

Glasco	US 2005/0251626 A1	Nov. 10, 2005 (filed on Apr. 24, 2003)
Rowlands	US 2003/0217236 A1	Nov. 20, 2003 (filed on Oct. 11, 2002)
Arimilli	US 6,138,218	Oct. 24, 2000 (filed on Feb. 17, 1998)

REJECTIONS

The Examiner rejects the claims as follows:

R1: Claims 1-4, 9, 14, 16, 17, 20, 23, 24, and 29 stand rejected under 35 U.S.C. § 102(e) for being anticipated by Glasco.

R2: Claims 5, 6, 10, 11, 13, 15, 18, 19, 21, 22, 25-28 and 30 stand rejected under 35 U.S.C. § 103(a) for being obvious over Glasco in view of Rowlands.

R3: Claims 7 and 12 stand rejected under 35 U.S.C. § 103(a) for being obvious over Glasco in view of Rowlands further in view of Arimilli.

Groups of Claims:

Claims will be addressed in the order of the arguments.

Appellants contend that the claimed subject matter is not anticipated by Glasco or rendered obvious by Glasco in combination with Rowlands or Arimilli or both for failure of the references to teach the computer system as

claimed. The Examiner contends that each of the claims is properly rejected.

Rather than repeat the arguments of Appellants or the Examiner, we refer to the Briefs and the Answer for their respective details. Only those arguments actually made by Appellants have been considered in this opinion. Arguments that Appellants could have made but chose not to make in the Briefs have not been considered and are deemed to be waived.

We affirm-in-part.

ISSUE

The principal issue before us is whether Appellants have shown that the Examiner erred in rejecting the claims under 35 U.S.C. § 102(e) and 35 U.S.C. § 103(a). The issue turns on whether Glasco teaches the notification of the ordering point migrating from the processor's cache to memory as claimed.

FINDINGS OF FACT

The record supports the following findings of fact (FF) by a preponderance of the evidence.

1. In a computer system, the "ordering point", sometimes called a "serialization point" is the place in the computer where the system goes to get the current, authoritative value of a variable (Spec. 3, ¶ [0019]). In a simple computer, the ordering point is the memory location where the variable is stored. If the computer has a processor with a cache memory, then for increased speed the processor may deposit a newly calculated value of the variable into its cache memory and delay the "writing back" of the value to the real memory location

until later (Spec. 1-2, ¶ [0003]). Until the write back, the memory location has "wrong" data in it, as the correct value is currently in the cache. This is called a "coherency" problem. During this time, the ordering point is the cache, as it contains the correct value of the variable. After the write back of the correct value from the cache to memory, the ordering point will migrate back to the memory (Spec. 2, ¶ [0004]).

2. Appellants have invented a system and method for indicating by a broadcast of a message to the system at large that the correct location to get the current value of a variable has moved from a cache memory to the system memory (Spec. 2, ¶¶ [0005], [0007]). That correct location, known as the ordering point or serialization point, may be first placed by the CPU in its cache memory, and later moved to the system memory (Spec. 1, ¶ [0003]; 3, ¶ [0019]). That movement would trigger the broadcast, so the other nodes of the network know where to find the value of the variable (Spec. 2, ¶ [0006]).

3. Glasco teaches the use of a cache coherence controller (CCC) to maintain coherency between nodes in a multi-node system (¶ [0052]). As taught by Glasco, the CCC serves to represent other non-local clusters of nodes to the local node in maintaining coherency throughout the system (¶ [0063]). The CCC in the home cluster can act as a serialization point in place of the memory controller for a time until the CPU issues a "final source done" indication, unblocking the memory (¶¶ [0108], [0109]).

4. Other findings of fact are presented in the Analysis section with individual reference citations.

PRINCIPLES OF LAW

Appellants have the burden on appeal to the Board to demonstrate error in the Examiner's position. *See In re Kahn*, 441 F.3d 977, 985-86 (Fed. Cir. 2006) ("On appeal to the Board, an applicant can overcome a rejection [under § 103] by showing insufficient evidence of prima facie obviousness or by rebutting the prima facie case with evidence of secondary indicia of nonobviousness.") (quoting *In re Rouffet*, 149 F.3d 1350, 1355 (Fed. Cir. 1998)).

"In reviewing the [E]xaminer's decision on appeal, the Board must necessarily weigh all of the evidence and argument." *In re Oetiker*, 977 F.2d 1443, 1445 (Fed. Cir. 1992).

In rejecting claims under 35 U.S.C. § 102, "[a] single prior art reference that discloses, either expressly or inherently, each limitation of a claim invalidates that claim by anticipation." *Perricone v. Medicis Pharm. Corp.,* 432 F.3d 1368, 1375 (Fed. Cir. 2005) (citation omitted).

"This court has held in a number of decisions that a United States patent speaks for all it discloses as of its filing date, even when used in combination with other references." *In re Zenitz*, 333 F.2d 924, 926 (CCPA, 1964) (internal citations omitted).

"It is not the function of [the U.S. Court of Appeals for the Federal Circuit] to examine the claims in greater detail than argued by an appellant, looking for nonobvious distinctions over the prior art." *In re Baxter Travenol Labs.,* 952 F.2d 388, 391 (Fed. Cir. 1991). Similarly, it is not the

function of this Board to examine claims in greater detail than argued by an appellant, looking for distinctions over the prior art.

ANALYSIS

From our review of the administrative record, we find that the Examiner has presented a prima facie case for the rejections of Appellants' claims under 35 U.S.C. §§ 102 and 103 on pages 3-10 of the Examiner's Answer. In opposition, Appellants present a number of arguments.

Arguments with respect to the rejection of claims 1 to 4, 9, 14, 16 to 17, 20, 23, 24, and 29 under 35 U.S.C. § 102(e) [R1]

Claim 1 will be representative of this group, which includes all of the independent claims 1, 9, 16 and 23.

Appellants' claim requires that a "write back" message be broadcast from a first node to at least one other node in the system when an acknowledgement is received indicating that the ordering point has migrated from the first node to the memory (Claim 1). In this context, a node is a processor including its cache. (*See* Spec., Fig. 1, #12, #22.) The claimed "write back message" is a message broadcast to at least one other node indicating that in the first node an acknowledgement was received from system memory stating that the memory received its new value from the cache, it's contents are now up-to-date, and it can now be the ordering point (Spec. 7, ¶ [0031]).

The Examiner cited Glasco as his main reference. Glasco teaches a multi-node computer system (Fig. 1B, #131) which relies on switching to reduce the inter-processing linkage and teaches a Cache Coherence Controller (CCC) #230 for providing the caching needs of the processors

and connections to the processors in remote clusters (Fig. 2; ¶ [0043]). Data coherency is also the responsibility of the CCC and the memory controllers. The serialization point, the same thing as the ordering point, provides the accurate data for nodes when required (¶ [0045]). When data is needed from, or sent to a remote cluster, the CCC acts as an aggregate remote cache and probing agent and represents the non-local nodes in local transactions where information must be sent to nodes outside of the local cluster (¶¶ [0070], [0071]).

In figure 13 of Glasco, we find examples of data being read from and sent to the CCC of remote clusters. In the example starting in ¶ [0108], to maintain cache coherency the CCC acts as the serialization point, bypassing the memory controller. That status will be maintained "until a final source done" message is received from the other cluster, the request cluster (¶ [0108]). The CCC of the remote cluster probes its nodes and "sends a response with a completion indicator to the request cluster 1300." (¶ [0108]). This process can be read on the claimed "acknowledgement provided by the memory", as the CCC is acting on behalf of the blocked memory controller. Finally, the CPU of the request cluster sends a "source done" message, which unblocks the memory line. Note in ¶ [0109] "At 1417, the memory line is unlocked after receiving a [']source done['] from the request cluster." (*See* ¶ [0109], ll. 13, 14.) The "source done" message is read on the claimed "write back message" as it indicates that the memory line can now provide updated data, as the claimed ordering point.

Appellants argue in the Brief (p. 17, bottom) and the Reply (p. 5, bottom) that "Glasco fails to disclose that an ordering point can migrate from a node to memory, as recited in claim 1." We find that the serialization point in Glasco does migrate: In ¶ [0108], the CCC 1321-1 in the home

cluster acts as a serialization point to maintain coherency (¶ [0108], l. 1). This lasts until a "final source done" command is received from the request cluster (*Id*).

Appellants argue that Glasco cannot disclose broadcasting a "write back message" by the first node (App. Br. 18, bottom). We read the "source done" message, as taught by Glasco (¶¶ [0108], [0109]), on the claimed "write back message", as it indicates the completion of the writing of the data to memory (¶[0108], ll. 7-11).

We thus do not find error in the rejection of claim 1.

Claim 2: Glasco teaches a cache coherence controller rather than a cache with a plurality of cache lines (App. Br. 19, middle). Appellants also argue that Glasco fails to disclose that a cache line has an associated state defining the cache ordering point for the data, with which we agree. Thus, we find claim 2 to be rejected in error.

Claim 3: Appellants argue that Glasco fails to disclose one other node providing a response to the broadcast write back message (App. Br. 20, middle). We agree, as the Examiner has not pointed out, and we do not find, a response to the write back message (source done message). Thus, we find claim 3 to be rejected in error.

Claims 4 is dependent on claim 3, and thus is also rejected in error.

Claim 9: Appellants argue that Glasco does not teach providing a response to the broadcast write back message (App. Br. 22, bottom). For the same reason expressed for claim 3, we find claim 9 to be rejected in error.

Claim 14 is dependent on claim 9, and thus is also rejected in error.

Claim 16 engenders the same analysis as claim 1, and thus we do not find error in the rejection of claim 16.

Claim 17 and 20: We find error in the rejection of these claims for the reasons expressed by Appellants (App. Br. 24, bottom).

Claim 23: Appellants argue that claim 23 has been rejected in error (App. Br. 25, top). For the same reasons expressed for claim 1, we decline to find error in the rejection.

Claim 24: Appellants argue that Glasco fails to disclose providing a response from the recipients of the broadcast (App. Br. 25, bottom). We agree, and therefor find error in the rejection.

Claim 29: Appellants present the same argument as for claim 2, and we agree (App. Br. 26, bottom). We thus find error in this rejection.

Arguments with respect to the rejection of claims 5, 6, 10, 11, 13, 15, 18, 19, 21, 22, 25 to 28 and 30 under 35 U.S.C. § 103(a) [R2]

Claims 5, 6, 10, 11, 13, 15, 18, 19, 21, 22, 25-28 and 30 stand rejected under 35 U.S.C. § 103(a) for being obvious over Glasco in view of Rowlands. Rowlands is cited for teaching the third node retrying the source broadcast request in an analogous art, as claimed (Ans. 6, middle).

Claim 5: Appellants argue the reasoning for claim 1, plus that Rowlands "simply discloses an interconnect that may or may not support retry of an address transfer (See Rowlands, Par. [0113])." (App. Br. 27, bottom). We find that Rowlands teaches the actual retry for coherency purposes. (¶ [0057]; ¶ [0113], l. 6), not just the support thereof (Ans. 26, bottom; 27, top). We note in passing that Appellants have not argued for this claim any features of parent claims 3 or 4, which arguments are therefore waived. Thus Appellants have not shown error in this rejection.

Claim 6: Appellants argue that Glasco has no teaching of recognizing a conflict, as required by the claim (App. Br. 28, middle). The Examiner points to ¶ [0137] of Glasco, in which remote and local coherency agents handle conflicts in the data when the data is conflicting. Thus, Appellants have not shown error in the rejection.

Claim 10 is dependent on claim 9, the rejection of which under 35 U.S.C. § 102 we have found to be in error. We find Rowlands does not cure the deficiencies Glasco as discussed for the rejection of claim 9. Thus, claims 10, 11, 13 and 15 are also rejected in error, albeit under a different statutory basis, 35 U.S.C. § 103(a).[2]

Claim 18 is argued by Appellants to be patentable for the same reasons as parent claim 17 (App. Br. 32, top). We agree, and find error in the rejection.

Claim 19 is argued by Appellants to be patentable for the same reasons as claim 16 and because the references fail to teach the means for recognizing a conflict (App. Br. 33, top). The rejection of claim 16 was found to be without error, so no deficiency is extant. Rowlands teaches a retry for coherency reasons, which are indicative of a conflict (¶ [0113]).

Claim 21, Appellants argue that claim 21 is dependent on claim 20 and is allowable for at least that reason and that Rowlands does not cure the deficiency of the Glasco reference as argued for the rejection of claim 20 (App. Br. 31, middle). We agree with Appellants and find claim 21 was rejected in error.

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[2] Appellants appear to argue that claim 13 is dependent on claim 8, found by the Examiner to be allowable (App. Br. 30, bottom). We find that claim 13 as presented to this tribunal is dependent on claim 9, not 8 (See App. Br. 42, and Spec. 26, top).

Claim 22, Appellants argue, is patentable because Rowlands fails to make up the deficiencies in the Glasco reference (App. Br. 33, bottom). Since we did not find Glasco deficient, this argument is not persuasive. Thus, we will not find error in the rejection.

Claims 25 and 26 are argued by Appellants to be patentable for the same reasons presented for claim 24 and that Rowlands does not make up for the deficiencies in Glasco (App. Br. 34, top). We agree and find error in the rejection of claims 25 and 26.

Claims 27 and 28 are argued by Appellants to be patentable because Rowlands does not make up for the deficiencies in Glasco and for the failure of each to recognize a conflict (App. Br. 34, 35). As mentioned for claim 5, we find that the combination of references teaches the recognition of conflict (Glasco, ¶ [0137]). We thus do not find error in the rejection of those claims.

Claim 30, it is argued by Appellants, is patentable for the same reasons as claim 29 (App. Br. 36, top). We agree and find error in the rejection of this claim.

Arguments with respect to the rejection of claims 7 and 12 under 35 U.S.C. § 103(a) [R3]

Claims 7 and 12 stand rejected under 35 U.S.C. § 103(a) for being obvious over Glasco in view of Rowlands and further in view of Arimilli.

Appellants argue that claim 7 is rejected in error as the Arimilli reference does not employ a forward progress protocol (App. Br. 37, top).

We have reviewed the Examiner's arguments and the reference and agree with Appellants. The same reasoning applies to the rejection of claim 12.

We thus find error in the rejections [R3] of claims 7 and 12.

CONCLUSIONS OF LAW

Based on the findings of facts and analysis above, we conclude that the Examiner erred in rejecting claims as follows:

R1: The following claims were rejected in error under 35 U.S.C. § 102: 2, 3, 4, 9, 14, 17, 20, 24, and 29. Claims 1, 16 and 23 were not found to be rejected in error.

R2: The following claims were rejected in error under 35 U.S.C. § 103: 10, 11, 13, 15, 18, 21, 25, 26 and 30. Claims 5, 6, 19, 22, 27 and 28 were not found to be rejected in error.

R3: Claims 7 and 12 were rejected in error.

DECISION

The Examiner's rejections [R1], [R2] and [R3] respectively of claims 2-4, 7, 9-15, 17, 18, 20, 21, 24-26, 29 and 30 are reversed. The rejections of claims 1, 5, 6, 16, 19, 22, 23, 27 and 28 are affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED-IN-PART

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